WHAT IS CLAIMED IS:

1. A data path circuit in a digital processing device, wherein the data path circuit is coupled to a memory bus for obtaining values from a memory, the data path circuit comprising

a first plurality of data lines;

a first data address generator for coupling the first plurality of data lines to the memory bus so that a value from the memory transferred by the memory bus can be placed onto the first plurality of data lines;

one or more functional units for performing a digital operation coupled to the plurality of data lines; and

a register coupled to the first plurality of data lines, wherein the register selectively stores a value from the first plurality of data lines so that the value is selectively available on the first plurality of data lines.

2. The data path circuit of claim 1, wherein the register includes a register file for selectively storing multiple values from the first plurality of data lines and for selectively applying the stored multiple values to the first plurality of data lines.

3. The data path circuit of claim 1, further comprising

a control signal coupled to the register for controlling storage of a value from the first plurality of data lines.

4. The data path circuit of claim 1, wherein a data field is used to select loading of a value on the memory bus of selectable bit width.

5. The data path circuit of claim 1, further comprising

a second plurality of data lines;

a second data address generator for coupling the second plurality of data lines to the memory bus so that a value from the memory transferred by the memory bus can be placed onto the second plurality of data lines; and

wherein the second data address generator is responsive to a control signal for selectively providing a data value from the first plurality of data lines to the second plurality of data lines.

6. A data path circuit in a digital processing device, wherein the data path circuit is coupled to a memory bus for obtaining values from a memory, the data path circuit comprising

a plurality of groups of data lines;

a plurality of data address generators for coupling the plurality of groups of data lines to the memory bus so that a value from the memory transferred by the memory bus can be placed onto a group of data lines;

one or more functional units for performing a digital operation coupled to the plurality of groups of data lines; and

a plurality of registers coupled to each group of data lines on a one-to-one correspondence, wherein the plurality of registers selectively store values from the plurality of groups of data lines so that the values are selectively available on the plurality of groups of data lines.

7. The data path circuit of claim 6, wherein 8 groups of 16 data lines are used, wherein each group of data lines is coupled to a register file capable of storing 8 16-bit words, wherein each of the data address generators can selectively provide a value on a first group of data lines to a second group of data lines.

8. The data path circuit of claim 1, wherein the functional units include a multiplier and accumulator, the data path circuit further comprising

a coupling of the multiplier to the plurality of data path lines;

a coupling of the accumulator to the plurality of data path lines;

direct data lines coupled between the multiplier and the accumulator.

9. The data path circuit of claim 8, wherein the direct data lines are uni-directional for transferring data from the multiplier to the accumulator.

10. A digital processing system comprising

a multiplier;

an accumulator;

a configurable data path coupled to the multiplier and the accumulator; and

a direct data path coupled between the multiplier and the accumulator.